REMARKS/ARGUMENTS

Rejections of Claims 1-27 under 35 U.S.C. 102(e):

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang et al. (U.S. 20030096486 A1).

Chuang discloses a self-aligned bipolar transistor with

(1); (7); (14); (21) a substrate (18):

a dielectric layer (19) formed on the substrate (18);

an opening (23) formed in the dielectric layer (19) to expose a portion of the substrate (18) (see Figures 2A-2H);

a semiconductor layer (24) formed on a sidewall and a bottom of the opening (23), the semiconductor layer extending (24) outside the opening (23) and above the dielectric layer (19) (see Figures 2A-2H);

a spacer (25) formed on the semiconductor layer (24) to define a self-aligned emitter region in the opening (23);

an emitter conductivity layer (26) being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer (26) and the semiconductor layer (24) (see Figures 2A-2H);

a salicide layer (27) formed on the emitter conductivity layer (26) and on the portion of the semiconductor layer (24) extending outside the opening (23) and above the dielectric layer (19) (see Figures 2A-2H);

(2) wherein the semiconductor layer comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs (see Figures 2A-2H);

(3) further comprising a selective implant collector region formed in the substrate beneath the semiconductor layer (see Figures 2A-2H);

(4) further comprising an extended conductivity layer formed on the dielectric layer

to connect to the semiconductor layer (see Figures 2A-2H);

(5) further comprising and oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer (see Figures 2A-2H);

(6); (13); (27) wherein the extended conductivity layer is composed of polysilicon (see Figures 2A-2H);

(8) further comprising a selective implant collector region formed in the substrate beneath the GaAs layer (see Figures 2A-2H).

Response:

According to the rejection reasons of claims 1-8, 13-14, 21, and 27 (as shown above) cited on pages 2-4 of the above identified Office action, this application is anticipated by Chuang's disclosure (US 20030096486) because he teaches the same bipolar transistor structure, having a semiconductor layer 24 on a sidewall and a bottom of the opening 23 of a dielectric layer 19, shown in Figs. 2A-2H. However, *there is no elements 19, 23, 24, 26-27 in figures of Chuang's application, and the elements in Chuang's figures does not correspond those elements mentioned by Examiner.* In addition, Chuang's application has been the cited reference in a previous Office action mailed on 05/03/2006, and applicant has filled a response to the previous Office action on 08/03/2006. Therefore, it is obviously that the Chuang's application should not be the cited reference mentioned by Examiner in the rejection reasons of this Office action (mailed on 10/20/2006). The argument for the patentability of this application when regarding to Chuang's application could be seen in the attachment sheets, the response to the Office action on 05/03/2006 (mailed on 08/03/2006). Applicant believes that this application should be allowable in consideration to Chuang's application.

When referring to the "Notice of References Cited" sheet attached with the above identified Office action, applicant fund that the patent US 4,800,176 (by Kakumu et al.) were cited and which had Figs. 2A-2H with elements 23-24, and 29. Therefore, applicant

confidently assumes it is Kakumu's application that is mentioned by Examiner in the above listed rejection reasons. Therefore, applicant will discuss the characteristics and differences of this application and Kakumu's application as following descriptions.

(1) Claim 1:

For clearly showing the characteristics of this application, claim 1 is listed as below:

"1. A bipolar junction transistor, comprising:

a substrate;

a dielectric layer formed on the substrate;

an opening formed in the dielectric layer to expose a portion of the substrate;

a semiconductor layer formed on a sidewall and a bottom of the opening, the semiconductor layer extending outside the opening and above the dielectric layer;

a spacer formed on the semiconductor layer to define a self-aligned emitter region in the opening;

an emitter conductivity layer being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer; and

a salicide layer formed on the emitter conductivity layer and on the portion of the semiconductor layer extending outside the opening and above the dielectric layer."

Accordingly, a **semiconductor layer 106** (referring to Fig.14) is limited in claim 1, which is formed on a sidewall and a bottom of the opening 98. The semiconductor 106 may be formed of group IIIA-VA compounds (para. [0028]). In addition, *since the spacer 106 is only formed on the sidewall surface of the opening 98, but not on the bottom of the opening 98, the emitter conductivity layer 108 filled in the self-aligned emitter region directly contacts the semiconductor layer 103 on the bottom of the opening 98 so as to form a* ***PN junction*** *between the emitter conductivity layer 108 and the semiconductor*

layer 103, which is also described in claim 1.

Referring to Kakumu's application, he discloses a fabrication process of a contact structure between a conductive wire and a heavily doped region in a semiconductor substrate. As shown in Figs.2A-2H, the isolation layer 19 is used as a mask to form an N-type high impurity concentration layer 21 in the P-type substrate 18 through the opening 23. Then, the oxide layer 22 and the polysilicon layer 24 are successively formed on the substrate 18. *Arsenic (As) or boron (B) is then ion-implanted into the polysilicon layer 24 (Col. 3, lines 49-59)*. An oxidization process is carried out to form an oxide layer 25 on the doped polysilicon layer 24. After that, a polysilicon layer 26 is formed in the opening 23 (Fig.2E) for planarizing the surface of the substrate 18. The exposed oxide layer 25 is then removed, and an Al-Si or Al conductive layer 27 is formed on the substrate 18 for forming a conducive wire after an etching process. Wherein, *the conductive wire (wire layer) shown in Fig.2H contains the Al-Si conductive layer 27 and the polysilicon layer 24 (Col.4, lines 13-15), and the doped polysilicon layer 24 may act as a diffusion source, too (Col.4, line 29).* ***Therefore, the doped polysilicon layer 24 is a conductive layer but not a semiconductor layer*** *limited in claim 1 of this application.*

Furthermore, *the oxide layer 25 of Kakumu's is formed on the surfaces of the bottom and the sidewall of the opening 23,* thus *it separates the polysilicon layer 26 and the doped polysilicon layer 24.* In this situation, *there is no PN junction occurring* in Kakumu's structure because the two polysilicon layers 24, 26 do not contact with each other at all. Accordingly, *Kakumu never discloses the PN junction claimed in claim 1 of this application.*

Since Kakumu's application does not teach all the limitations in claim 1 of this application, such as the PN junction and semiconductor layer, claim 1 should be pantentable regarding to USC 102(e). Reconsideration of claim 1 is politely requested.

(2) Claims 7, 14, 21:

Claims 7, 14, and 21 are similar to claim 1, and the main differences between those claims and claim 1 are that the semiconductor layer is replaced by a GaAs layer, InP layer, or a AlGaAs layer respectively in claims 7, 14, and 21 (para. [0028], line 6). *Since Kakumu never teaches his doped polysilicon layer 24 may be replaced by GaAs, InP, or AlGaAs materials, Kakumu's disclosure does not disclose all the characteristics of claims 7, 14, and 21, such as the PN junction, as described in above section (1), and these semiconductor materials.* Therefore, claims 7, 14, and 21 should be allowable. Reconsideration of claims 7, 14, and 21 is respectfully requested.

(3) Claim 2:

According to claim 2, the semiconductor layer comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs. However, *Kakumu never teaches or suggests its doped polysilicon layer 24 may be replaced by silicon epitaxy, GaAs, InP and AlGaAs materials*, thus claim 2 of this application should be allowable. Reconsideration of claim 2 is politely requested.

(4) Claims 3 and 8:

Claims 3 and 8 describe that the dipolar junction transistor further comprises a selective implant collector (SIC) region 102 positioned in the substrate 70, below the semiconductor layer 103 (or a GaAs layer). Referring to *Kakumu's application, he is silent on the SIC element and never suggests to form a SIC in the substrate 18 (Figs.2A-2H). Therefore, claims 3 and 8 should be allowable.* Reconsideration of claims 3 and 8 is respectfully requested.

(5) Claim 4:

Claim 4 of this application describes that the bipolar junction transistor further

comprises an extended conductivity layer 96 formed on the dielectric layer 84 to connect to the semiconductor layer 103. *Kakumu never teaches or suggests his structure further comprises an extended conductivity layer. In addition, there is no semiconductor layer disclosed in Kakumu's structure. Therefore, even there is an extended conductivity layer in Kakumu's structure, the extended conductivity layer or any other conductive layer still cannot connect to any semiconductor layer.* As a result, claim 4 of this application should be allowable. Reconsideration of claim 4 is politely requested.

(5) Claim 5:

Claim 5 claims that the dipolar junction transistor further comprises an oxide layer 92 and a silicon nitride layer 94 positioned between the extended conductivity layer 96 and the dielectric layer 84. According to Figs. 2A-2H of Kakumu's, there is a silicon oxide layer 22 positioned above the dielectric layer 19, but Kakumu does not teach any silicon nitride layer in his structure. As a result, Kakumu does not disclose all the limitations in claim 5 of this application, and claim 5 should be allowable. Reconsideration of claim 5 is politely requested.

(6) Claims 6, 13, and 27:

Claims 6, 13, and 27 describe that the material of extended conductivity layer 96 is polysilicon. Although the polysilicon layer 24 of Kakumu's disclosure may be regard as the extended conductivity layer 96, there is still no semiconductor layer in Kakumu's structure, which is claimed in claims 1, 7, 21. Since claims 6, 13, and 27 are dependent upon claims 1, 7, and 21 respectively, they should be allowable. Reconsideration of claims 6, 13, and 27 is requested.

(7) Claims 9-12, 15-20, and 22-26:

Examiner does not mention the rejection reasons of claims 9-12, 15-20, and 22-26, thus these claims should be allowable. In addition, Kakumu's application does not

disclose all the limitations in claims 9-12, 15-20, and 22-26, and these claims are dependent upon claims 1, 7, 14, and 21 so that they should be allowable if claims 1, 7, 14, and 21 are allowable. Reconsideration of claims 9-12, 15-20, and 22-26 is hereby requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)